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FDPC5030SG PowerTrench[®] Power Clip 30V Asymmetric Dual N-Channel MOSFET

Features

Q1: N-Channel

- Max r_{DS(on)} = 5.0 mΩ at V_{GS} = 10 V, I_D = 17 A
- Max r_{DS(on)} = 6.5 mΩ at V_{GS} = 4.5 V, I_D = 14 A

Q2: N-Channel

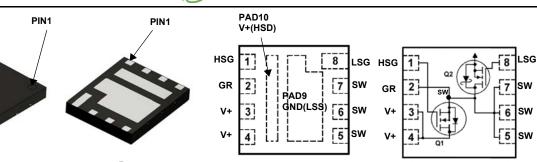
- Max r_{DS(on)} = 2.4 mΩ at V_{GS} = 10 V, I_D = 25 A
- Max $r_{DS(on)}$ = 3.0 m Ω at V_{GS} = 4.5 V, I_D = 22 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- RoHS Compliant

General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFETTM (Q2) have been designed to provide optimal power efficiency.

Applications

- Computing
- Communications
- General Purpose Point of Load



Top Power Clip 5X6 Bottom

Pin	Name	Description	Pin	Name	Description	Pin	Name	Description
1	HSG	High Side Gate	3,4,10	V+(HSD)	High Side Drain	8	LSG	Low Side Gate
2	GR	Gate Return	5,6,7	SW	Switching Node, Low Side Drain	9	GND(LSS)	Low Side Source

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parameter			Q2	Units	
V _{DS}	Drain to Source Voltage		30	30	V	
V _{GS}	Gate to Source Voltage		±20	±12	V	
	Drain Current -Continuous	T _C = 25 °C (Note 5)	56	84		
	-Continuous	T _C = 100 °C (Note 5)	35	53 25 ^{Note1b}	A	
ID	-Continuous	T _A = 25 °C	17 ^{Note1a}			
	-Pulsed	T _A = 25 °C (Note 4)	227	503	1	
E _{AS}	Single Pulse Avalanche Energy	(Note 3)	54	96	mJ	
	Power Dissipation for Single Operation	T _C = 25 °C	23 25			
P _D	Power Dissipation for Single Operation	T _A = 25 °C	2.1 ^{Note1a}	2.3 ^{Note1b}	W	
	Power Dissipation for Single Operation	T _A = 25 °C	1.0 ^{Note1c}	1.1 ^{Note1d}	1	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to	+150	°C	

Thermal Characteristics

$R_{ ext{ heta}JC}$	Thermal Resistance, Junction to Case	5.6	4.9	
R_{\thetaJA}	Thermal Resistance, Junction to Ambient	60 ^{Note1a}	55 ^{Note1b}	°C/W
$R_{ ext{ heta}JA}$	Thermal Resistance, Junction to Ambient	130 ^{Note1c}	120 ^{Note1d}	

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Device Marking		Device	Package Reel Size		Tape Width			Quantity		
FDPC5030SG FDPC5030SG		FDPC5030SG	Power Clip 56 13 "			12 mm			3000 units	
Electric	al Chara	cteristics T _J = 25 °C	unless otherwise note	ed.						
Symbol		Parameter	Test Cond	ditions	Туре	Min	Тур	Max	Units	
Off Chara	cteristics									
BV _{DSS}	Drain to Sc	ource Breakdown Voltage	I _D = 250 μA, V _{GS} = I _D = 1 mA, V _{GS} = 0		Q1 Q2	30 30			V	
ΔBV _{DSS} ΔTJ	Breakdown Coefficient	Voltage Temperature	$I_D = 250 \ \mu A$, refere $I_D = 10 \ mA$, referer		Q1 Q2		15 16		mV/°C	
I _{DSS}	Zero Gate	Voltage Drain Current	$V_{DS} = 24 V, V_{GS} = 0 V$ $V_{DS} = 24 V, V_{GS} = 0 V$		Q1 Q2			1 500	μΑ μΑ	
I _{GSS}	Gate to So Forward	urce Leakage Current,	$V_{GS} = 20 V, V_{DS} = 0$ $V_{GS} = 12 V, V_{DS} = 0$) V	Q1 Q2			100 100	nA nA	
On Chara	cteristics						II		1	
V _{GS(th)}		urce Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \ \mu A$ $V_{GS} = V_{DS}, I_D = 1 \ m A$		Q1 Q2	1.0 1.0	1.7 1.6	3.0 3.0	V	
$\frac{\Delta V_{GS(th)}}{\Delta T_{.1}}$		urce Threshold Voltage	$I_D = 250 \ \mu\text{A}, \text{ refere}$ $I_D = 10 \ \text{mA}, \text{ refere}$	nced to 25 °C	Q1 Q2	-	-5 -3		mV/°C	
			$V_{GS} = 10V, I_D = 17$ $V_{GS} = 4.5 V, I_D = 17$ $V_{GS} = 10 V, I_D = 17$	A 4 A	Q1		4.1 5.4 5.7	5.0 6.5 7.0		
r _{DS(on)}	Drain to Sc	ource On Resistance	$V_{GS} = 10V, I_D = 25 A$ $V_{GS} = 4.5 V, I_D = 22 A$ $V_{GS} = 10 V, I_D = 25 A, T_J = 125 °C$		Q2		1.9 2.4 2.7	2.4 3.0 3.4	mΩ	
9 _{FS}	Forward Tr	ansconductance	$V_{DS} = 5 V, I_D = 17 A$ $V_{DS} = 5 V, I_D = 25 A$		Q1 Q2		93 139		S	
Dynamic	Character	istics	55 5							
C _{iss}	Input Capa		Q1: V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHZ		Q1 Q2		1224 2730	1715 3825	pF	
C _{oss}	Output Cap	pacitance			Q1 Q2		397 801	560 1125	pF	
C _{rss}	Reverse Tr	ansfer Capacitance	Q2: V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHZ		Q1 Q2		42 72	60 100	pF	
R _g	Gate Resis	tance			Q1 Q2	0.1 0.1	0.5 1.1	1.5 2.2	Ω	
Switching	g Characte	eristics								
t _{d(on)}	Turn-On De	elay Time			Q1 Q2		8 10	16 19	ns	
t _r	Rise Time		Q1: V _{DD} = 15 V, I _D = 17	' Α, R _{GEN} = 6 Ω	Q1 Q2		2 4	10 10	ns	
t _{d(off)}	Turn-Off De	elay Time	Q2: V _{DD} = 15 V, I _D = 25	A Rock = 60	Q1 Q2		18 30	33 48	ns	
t _f	Fall Time		• UU - 10 •, I <u>D</u> - 20	GEN - 0.32	Q1 Q2		2 3	10 10	ns	
Qg	Total Gate	Charge	V_{GS} = 0 V to 10 V	Q1	Q1 Q2		17 39	24 55	nC	
Qg	Total Gate	Charge	V_{GS} = 0 V to 4.5 V		Q1 Q2		8 18	11 26	nC	
Q _{gs}	Gate to So	urce Gate Charge		Q2 V _{DD} = 15 V, I _D	Q1 Q2		3.1 6.1		nC	
Q _{gd}	Gate to Dra	ain "Miller" Charge		= 25 A	Q1 Q2		2.0 4.3		nC	

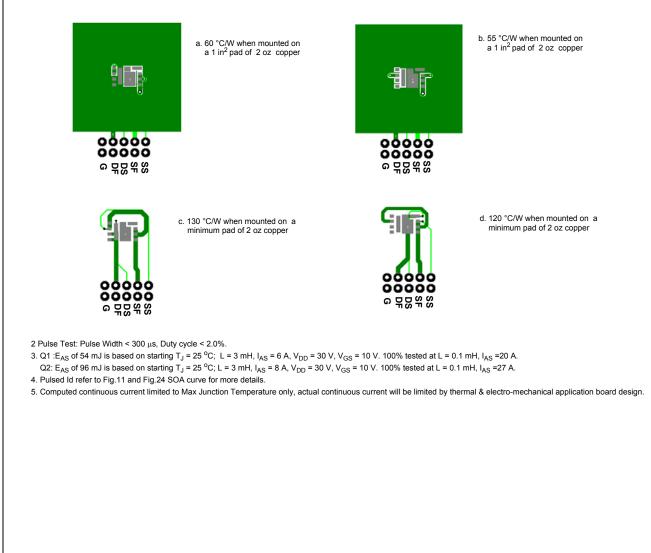
Package Marking and Ordering Information

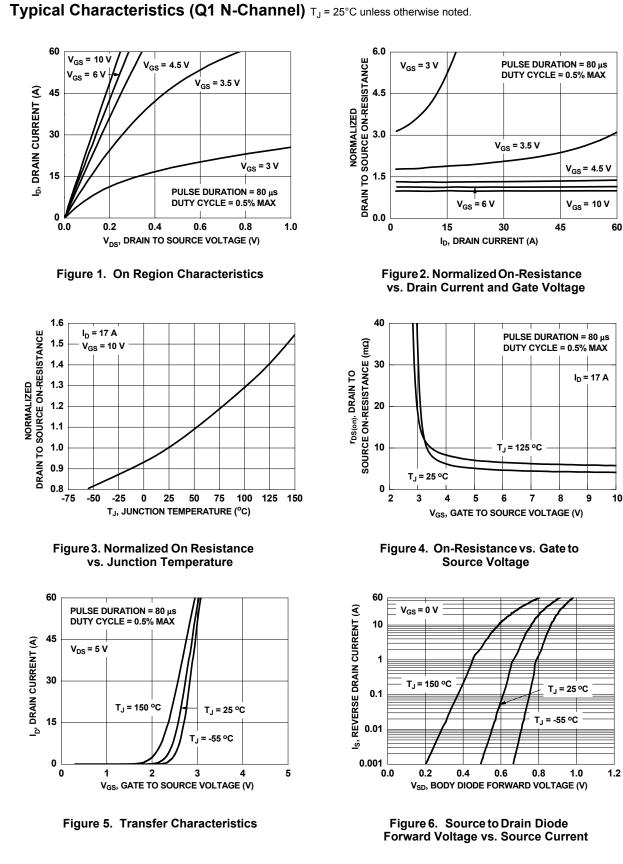
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Symbol	Parameter Test Conditions		Туре	Min	Тур	Мах	Units
Drain-Sou	urce Diode Characteristics						
V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 V, I_S = 17 A$ (Note 2 $V_{GS} = 0 V, I_S = 25 A$ (Note 2			0.8 0.8	1.2 1.2	V
t _{rr}	Reverse Recovery Time	Q1 I _F = 17 A, di/dt = 100 A/µs	Q1 Q2		23 27	37 44	ns
Q _{rr}	Reverse Recovery Charge	Q2 I _F = 25 A, di/dt = 230 A/µs	Q1 Q2		8 31	16 50	nC

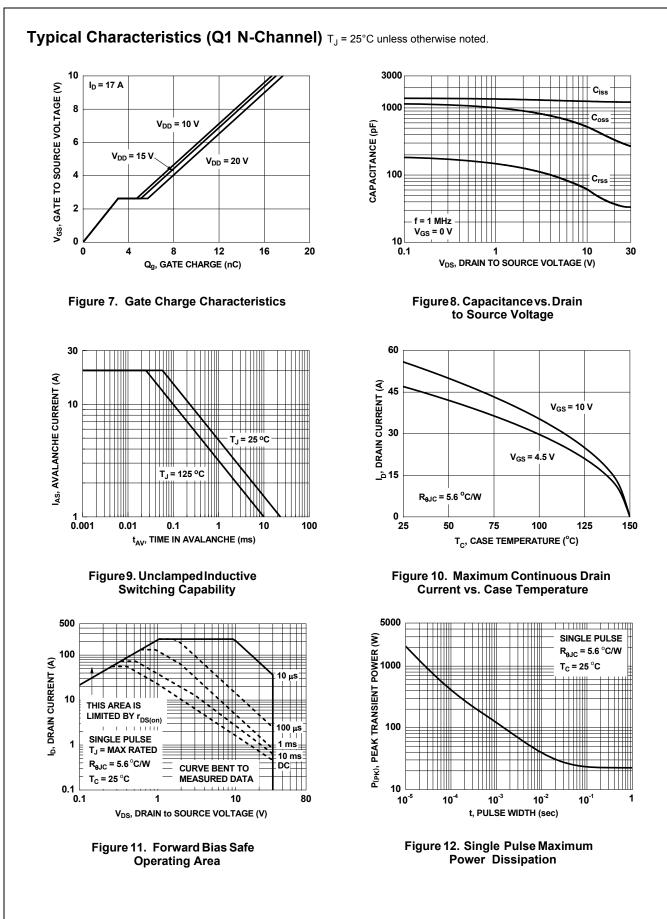
Notes:

 $1.R_{\theta,LA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material, $R_{\theta,CA}$ is determined by the user's board design.

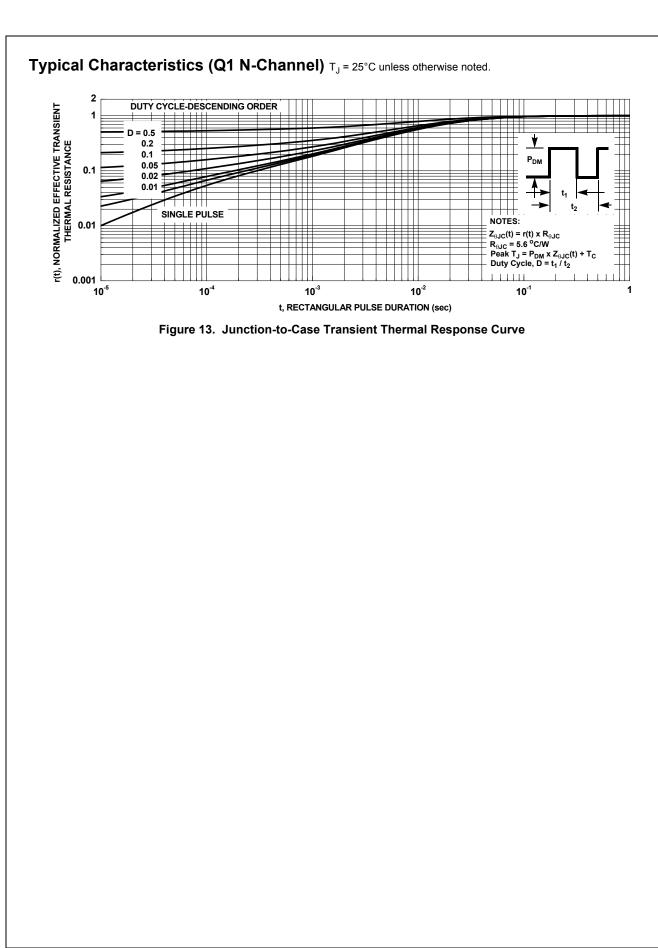


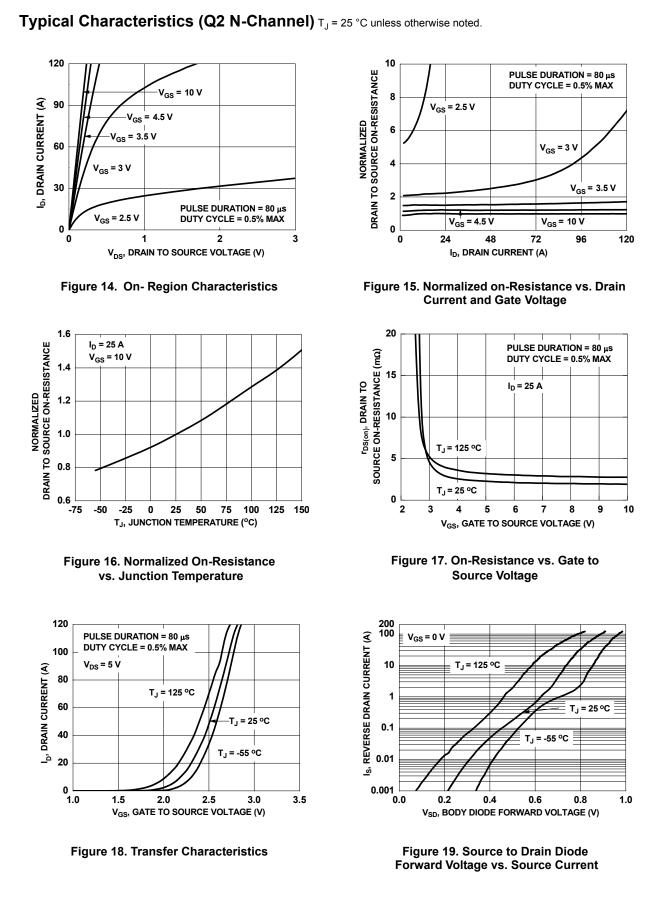


FDPC5030SG PowerTrench[®] Power Clip

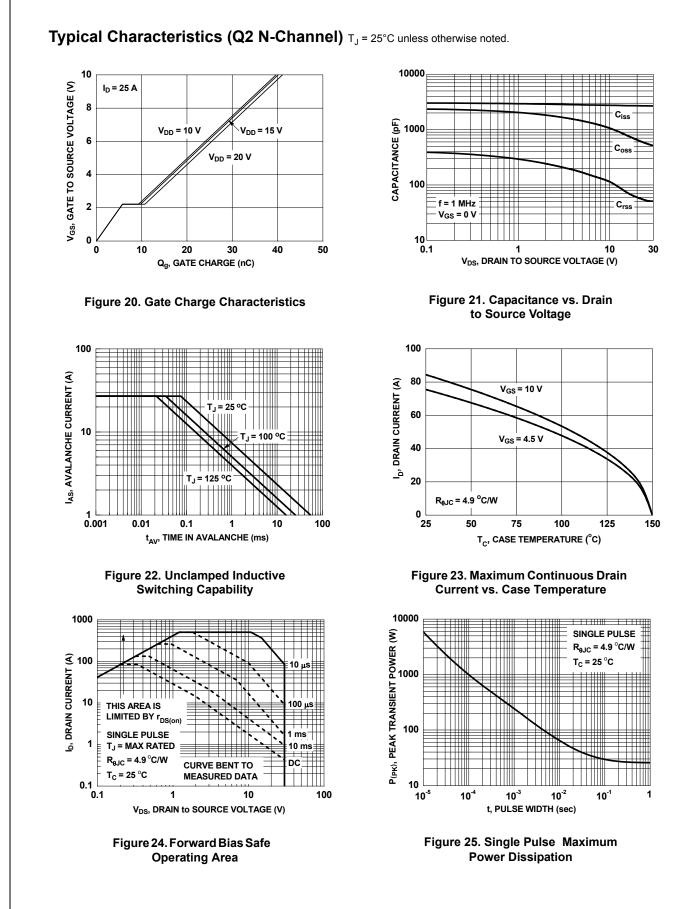




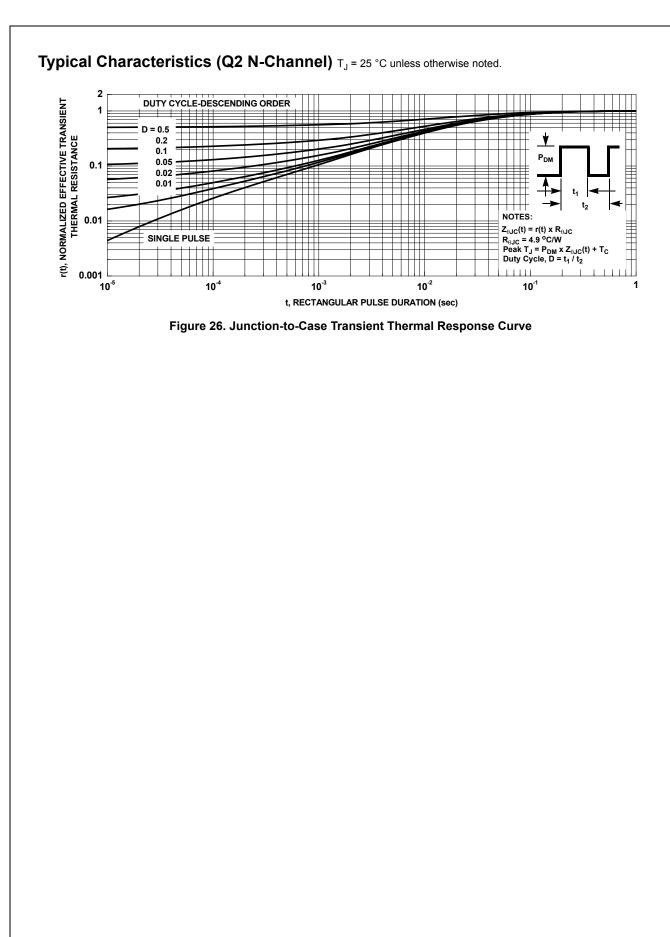




FDPC5030SG PowerTrench[®] Power Clip







Typical Characteristics (continued)

SyncFET[™] Schottky Body Diode Characteristics

Fairchild's SyncFETTM process embeds a Schottky diode in parallel with PowerTrench[®] MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC5030SG.

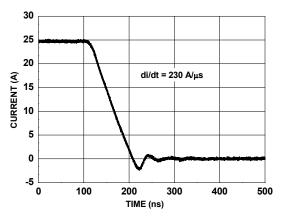


Figure 27. FDPC5030SG SyncFET[™] Body Diode Reverse Recovery Characteristic

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

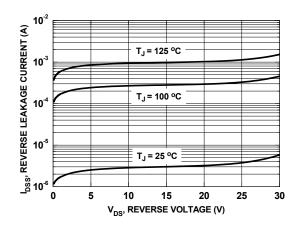
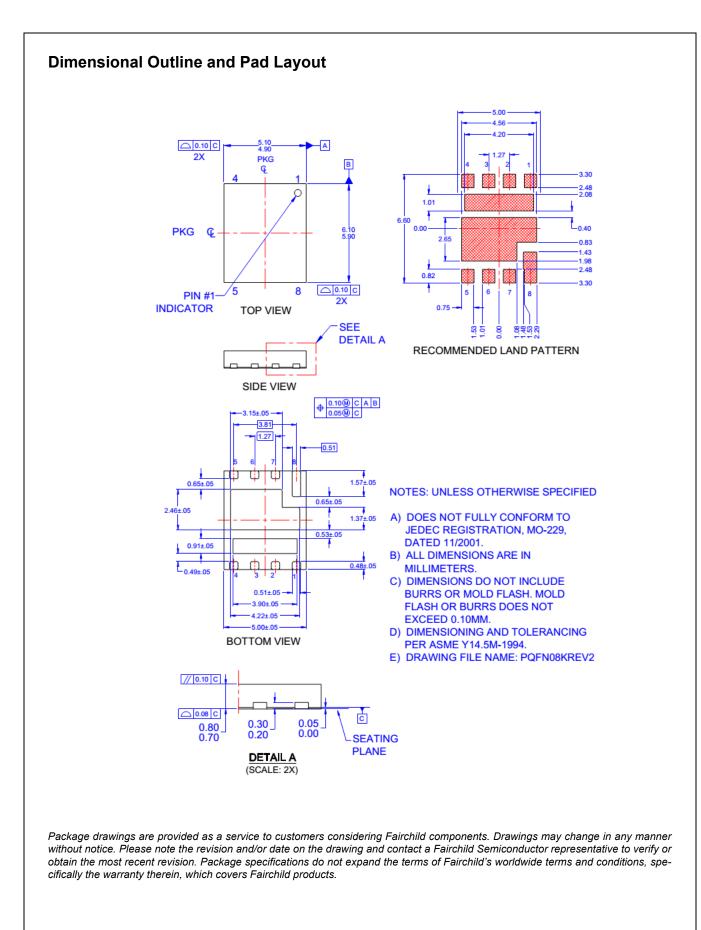


Figure 28. SyncFET[™] Body Diode Reverse Leakage vs. Drain-Source Voltage

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